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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/801,547 | 03/17/2004 | Masakazu Isomura | 119102 | 2324 |

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OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

| EXAMINER | |
|---|---|
| KIM, KENNETH S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2111 | |

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/801,547 | ISOMURA, MASAKAZU | |
| | Examiner | Art Unit | |
| | Kenneth S. KIM | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

KENNETH S. KIM
PRIMARY EXAMINER

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *Mar17'04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-11 are presented for examination.

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6, the description of predetermined element register is ambiguous with respect to the vector register comprising multiple element registers.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Demjanenko, U.S. Patent Application Publication No. 2004/0073773.

Demjanenko teaches the invention as claimed in claim 1 including a vector processor for processing vector data comprising multiple element data using a register, the vector processor comprising:

(a) a register usable as a vector register comprising multiple element registers (par. 668, line 5), and

(b) an addressing circuit for circularly specifying addresses of the vector register with the address of any element register of the vector register as the top (par.668, line 4), and

further teaches as in claims 2-5 and 7-11,

(c) the resister is a set of multiple scalar registers, and, by any of the scalar registers being specified as the top, the addresses of the multiple scalar registers are circularly specified (par. 668, line 5) – claim 2,

(d) the register comprises a vector register, any element register of the vector register being specifiable as the top.(par. 668, line 4) – claim 3, and

(e) when performing a vector operation on data stored in the register, element data of the vector register are sequentially read from the addresses of the vector register beginning with the address specified as the top, and reading of the element data is continuable by returning to the top address if the end address is reached (par. 668, line 5) – claims 4, 5, and 7-11.

The method claim 6 is equivalently rejected based on the same reason.

6. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hinds et al, U.S. Patent No. 6,189,094.

Hinds et al teaches the invention as claimed in claim 1 including a vector processor for processing vector data comprising multiple element data using a register, the vector processor comprising:

(a) a register usable as a vector register comprising multiple element registers (fig. 5), and

(b) an addressing circuit for circularly specifying addresses of the vector register with the address of any element register of the vector register as the top (col. 7, line 39), and

further teaches as in claims 2-5 and 7-11,

(c) the resister is a set of multiple scalar registers, and, by any of the scalar registers being specified as the top, the addresses of the multiple scalar registers are circularly specified (col. 7, lines 34 and 54) – claim 2,

(d) the register comprises a vector register, any element register of the vector register being specifiable as the top.(col. 7, line 49) – claim 3, and

(e) when performing a vector operation on data stored in the register, element data of the vector register are sequentially read from the addresses of the vector register beginning with the address specified as the top, and reading of the element data is continuable by returning to the top address if the end address is reached (col. 7, line 56) – claims 4, 5, and 7-11.

The method claim 6 is equivalently rejected based on the same reason.

7. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Izumisawa et al, U.S. Patent Application Publication No. 2004/0073773.

Izumisawa et al teaches the invention as claimed in claim 1 including a vector processor for processing vector data comprising multiple element data using a register, the vector processor comprising:

(a) a register usable as a vector register comprising multiple element registers (col. 4, line 48), and

(b) an addressing circuit for circularly specifying addresses of the vector register with the address of any element register of the vector register as the top (col. 4, line 46), and

further teaches as in claims 2-5 and 7-11,

(c) the resister is a set of multiple scalar registers, and, by any of the scalar registers being specified as the top, the addresses of the multiple scalar registers are circularly specified (col. 4, line 46) – claim 2,

(d) the register comprises a vector register, any element register of the vector register being specifiable as the top.(col. 4, line 43) – claim 3, and

(e) when performing a vector operation on data stored in the register, element data of the vector register are sequentially read from the addresses of the vector register beginning with the address specified as the top, and reading of the element data is continuable by returning to the top address if the end address is reached (col. 4, line 47 – claims 4, 5, and 7-11.

The method claim 6 is equivalently rejected based on the same reason.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cray taught a method of reading and writing to the same vector register.

Glossner III. et al taught a method of addressing vector register staring at an arbitrary address.

Fujii et al taught a method of using scalar registers as vector registers.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth S KIM whose telephone number is (571) 272-3627. The examiner can normally be reached on M-F (8:30-17:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for all communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

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April 13, 2006

KENNETH S. KIM
PRIMARY EXAMINER